**Test-Friendly Data-Selectable Self-Gating (DSSG)**

**Proposed Title**

* **Design and implementation of Post Silicon Validation for DFT**

**Abstract**

* **Clock networks consume large amounts of dynamic power,Clock gating is a common method for dynamic power reduction, and XOR self-gating is one of the useful clock gating methods for reducing meaningless clock toggling to provide extreme power reduction.**
* **In the Existing system, Design of test friendly architecture is evaluated in which the ATPG test is done using the data selectable self gating technique**
* **In the proposed system 4 types of Test pattern generation test is completely implemented. The test such as checker board test, pattern test, pseudorandom test., marching test have been evaluated to perform the post silicon validation completely.**

**Existing System**

* **In the Existing system, Design of test friendly architecture is evaluated in which the ATPG test is done using the data selectable self gating technique**

**Problem Statement**

* **Only selectable logics are tested**

**Proposed system**

* **In the proposed system 4 types of Test pattern generation test is completely implemented. The test such as checker board test, pattern test, pseudorandom test., marching test have been evaluated to perform the post silicon validation completely.**

**Solution Statement**

* **Four highly strong testing is performed.**
* **Benchmark circuit is tested after the ATPG**

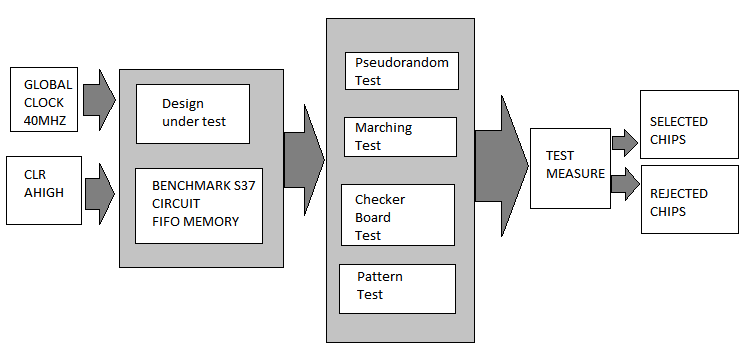
**Applications**

* **Bare chip Testing**
* **In built testing of FPGA**

**Software Used**

* **MODELSIM 6.3**
* **XILINX 12.5**

**Block Diagram**

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**MODULE DESCRIPTIONS**

**Module 1**

* **Design of Test pattern generation**
* **Pseudorandom test generation is the simplest method of creating tests. It uses a pseudorandom number generator to generate test vectors, and relies on logic simulation to compute good machine results, and fault simulation to calculate the fault coverage of the generated vectors.**

**Module 2**

* **Checker Board and Marching Test**
* **Alternate zeros and ones are written fast into the memory**
* **Fast read writes are performed in the fifo memory**

**Module 3**

* **Design of memory and Integration**
* **This module used to integrate the test pattern principles with the Memory module developed.**